

Enhanced Capture Timer Module



Reference Manual

ECT_16B8C

Block User Guide

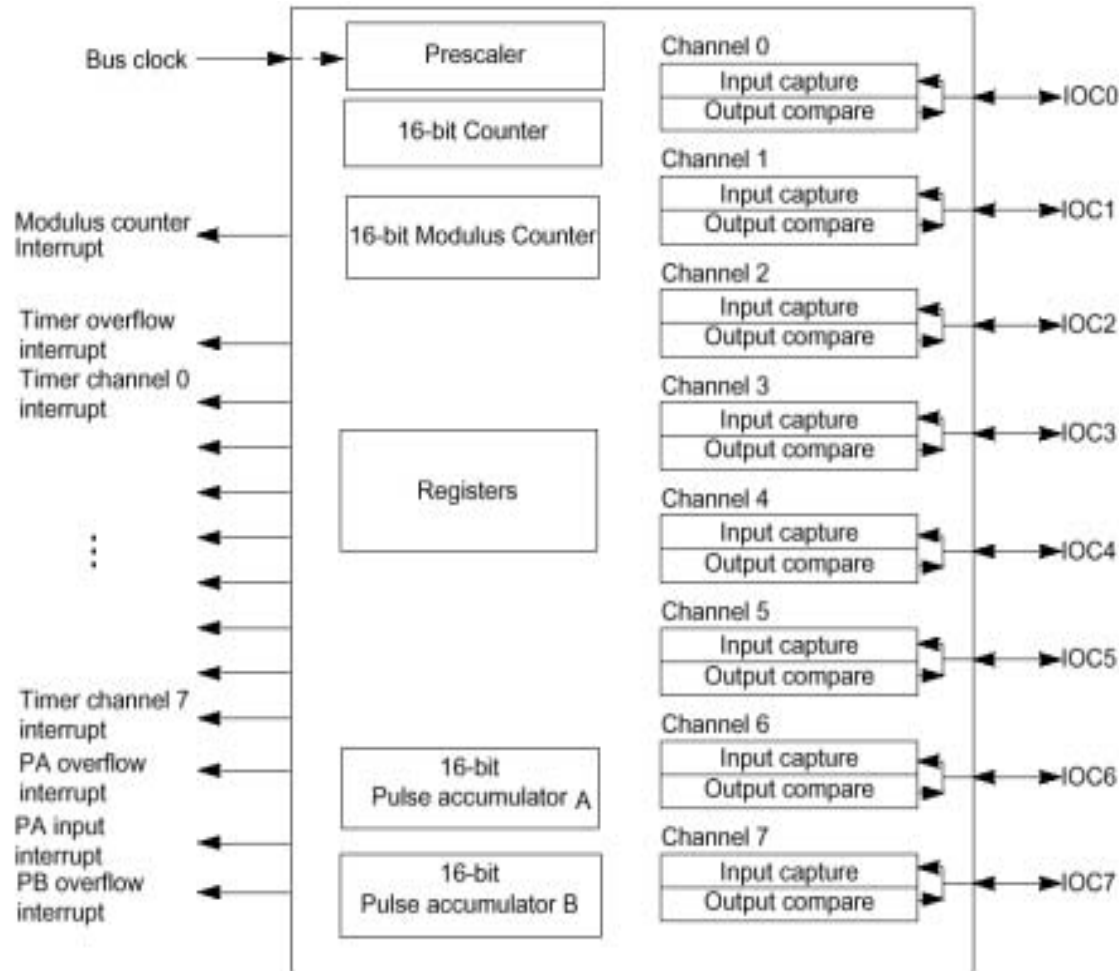
(Enhanced Capture Timer 16b buffered Reg. & 8b. counter)

ECT Hardware Overview

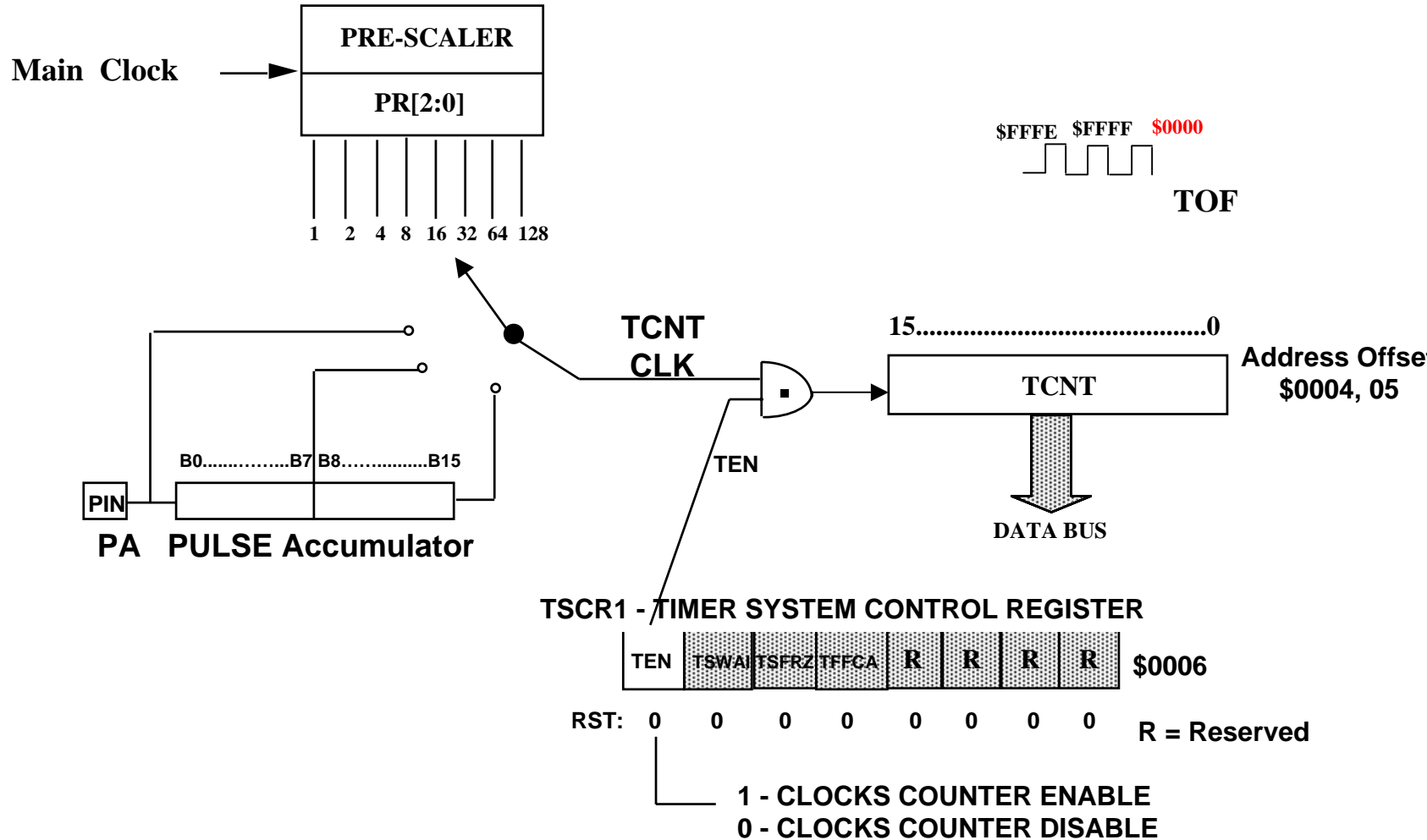
A 16-bit master up-counter & A 16-bit modulus down-counter ,with programmable prescaler.

8 independent timer channels, each capable of input capture and output compare functions.

4 x 8-bit pulse accumulators which maybe configured as 2 x 16-bit pulse accumulators.

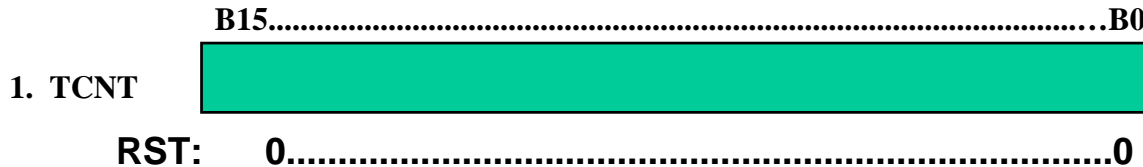


TIMER STRUCTURE

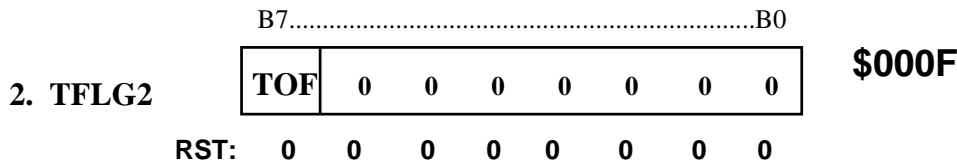


Timer, Prescaler and Counter

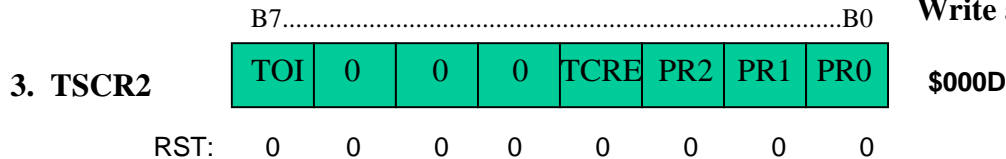
REGISTERS: 16 BIT FREE RUNNING /MODULO COUNTER



Address Offset
\$0004, \$0005



Timer Overflow Flag
Write a '1' to clear



1 - TIMER RESET BY OC7 MATCH
0 - COUNTER IS FREE RUNING

1 - TIMER OVERFLOW INTERRUPT ENABLE
0 - TIMER OVERFLOW INTERRUPT DISABLE

PRESCALER SELECTION

PR2	PR1	PR0	DIVIDE BY
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

TCRE - ALLOWS FOR PULSE
WIDTH MODULATION FUNCTION.

TIMER OPERATION

USEFUL FOR: 1. BASIS FOR ALL THE TIMING FUNCTIONS

2. PROVIDING TIME INFORMATION TO PROGRAMS

DESCRIPTION:

THE E-CLOCK DRIVES A PRESCALER, DIVIDE BY 1, TO 128, WHICH IN TURN DRIVES A 16 BIT COUNTER.

WHEN THE TIMER GOES FROM \$FFFF TO \$0000:

- THE TIMER OVERFLOW FLAG BIT IS SET IN ADDITION:**

- AN OVERFLOW INTERRUPT MAY OCCUR**

Timer Overflow Interrupt

INTERRUPT:

FOR TIMER OVERFLOW

- **TO CLEAR INTERRUPT WRITE 1 TO TOF BIT TFLG2.
DO NOT USE BIT MANIPULATION INSTRUCTIONS (SINCE RM/W OPERATION)**
- **TIMER OVERFLOW VECTOR USED.**

RESET CONDITIONS:

TCNT IS INITIALIZED TO ALL ZEROES AND Disabled

TIMER OVERFLOW INTERRUPTS ARE Disabled

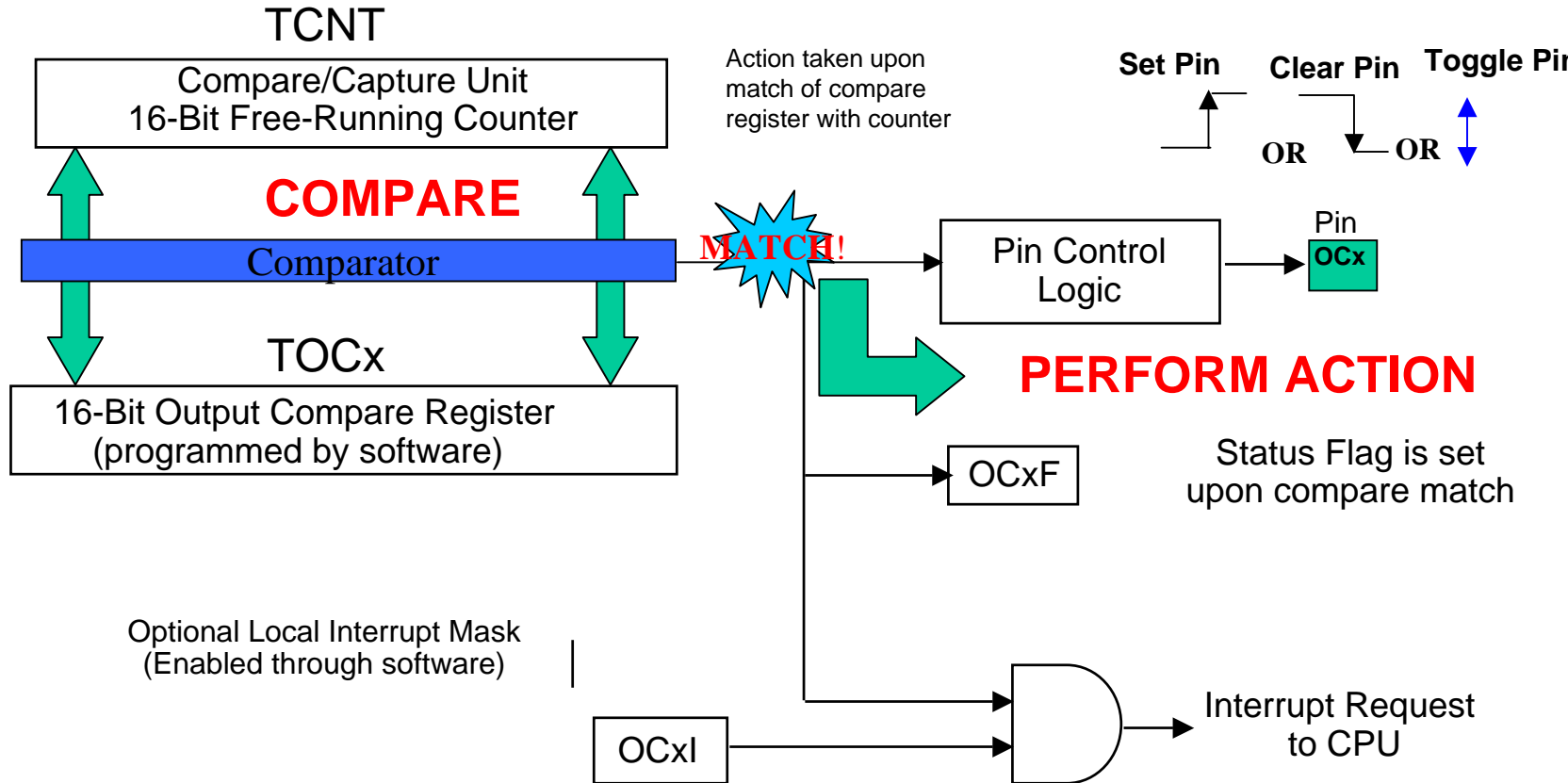
TC7 - TC0 REGISTERS ARE CLEARED

TIMER OVERFLOW FLAG IS CLEARED

PRESCALER IS 1

Output Compare Function

- Provides a mechanism to output a signal at a specific time



- UP TO 8 separate Output Compare Functions
- Each Output Compare Function has its own Vector and Controls

Output Compare, OC7-OC0

(1 of 4)

USEFUL FOR:

- 1. OUTPUT WAVEFORM CONTROL (SOFTWARE CONTROLLED)**
- 2. ELAPSED TIME INDICATOR (TO EXTERNAL CIRCUITRY)**

DESCRIPTION: DURING EACH E-CLOCK CYCLE, THE OUTPUT COMPARE REGISTERS ARE COMPARED TO THE FREE-RUNNING COUNTER.
IF THERE IS A COMPARE THEN:

- 1. THE INTERRUPT FLAG BIT IS SET**

IN ADDITION, EITHER OR BOTH OF THE FOLLOWING MAY OCCUR:

- 1. THE STATE OF THE ASSOCIATED OUTPUT PIN MAY BE CHANGED**

- 2. AN INTERRUPT IS GENERATED TO CPU, IF Enabled**

16 BIT CAPTURE COMPARE REGISTER (TC7)

\$0010 - \$0011

1. TC7 – TC0

16 BIT CAPTURE COMPARE REGISTER (TC0)

\$001E - \$001F

2. TFLG1

B7	B6	B5	B4	B3	B2	B1	B0
C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
RST: 0	0	0	0	0	0	0	0

\$000E

COMPARE/CAPTURE FLAGS
Write '1' to Clear Interrupt Flag

3. TIE

B7	B6	B5	B4	B3	B2	B1	B0
C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
RST: 0	0	0	0	0	0	0	0

\$000C

COMPARE/ CAPTURE MASK
0 = Interrupt Request Masked
1 = Interrupt Request Enabled

4. TCTL1

B7	B6	B5	B4	B3	B2	B1	B0
OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
RST: 0	0	0	0	0	0	0	0

\$0008

OUTPUT MODE AND
OUTPUT LEVEL (O7–OC0)

5. TCTL2

B7	B6	B5	B4	B3	B2	B1	B0
OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
RST: 0	0	0	0	0	0	0	0

\$0009

OMX	OLX	Action on OCx
0	0	No Action OCx
0	1	Toggle OCx
1	0	Drive OCx LO
1	1	Drive OCx HI

Force Output Compare

(3 of 4)

5. CFORC - FORCE OUTPUT COMPARE

	B7	B6	B5	B4	B3	B2	B1	B0	
	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0	\$0001
RST:	0	0	0	0	0	0	0	0	

PINS: 1. OC7–OC0 (PORT T PINS 7-0)

USED TO STABLISH INITIAL TIMER PIN STATES.

NOTE: FORCE OUTPUT COMPARE DOES NOT SET OC_x FLAGS.

FORCE OUTPUT COMPARE 7 MAY AFFECT ANY OR ALL OUTPUT COMPARE PINS.

Output Compare, OC7-OC0 (4 of 4)

INTERRUPTS: FOR OUTPUT COMPARES OC7-OC0

- TO CLEAR INTERRUPT, WRITE 1 TO OCxF BIT IN TFLG1
DO NOT USE BIT MANIPULATION INSTRUCTIONS (SINCE RM/W OPERATION)
- OC7-OC0 VECTORS ARE USED

RESET CONDITIONS:

- FREE RUNNING COUNTER (TCNT) INITIALIZED TO \$0000 AND Disabled.
- OUTPUT COMPARE REGISTERS ARE INITIALIZED TO \$0000
- OUTPUT COMPARE PINS ARE DISCONNECTED FROM OUTPUT COMPARE FUNCTIONS
- INTERRUPTS are Disabled
- FLAG BITS ARE CLEARED
- FORCE COMPARE BITS ARE CLEARED

Output Compare, OC7

(1 of 2)

- USEFUL FOR:
1. CONTROL OF MULTIPLE OUTPUT COMPARE PINS
 2. CONTROL OF A SINGLE PIN BY TWO OUTPUT COMPARES (THUS, SHORT PULSES ARE POSSIBLE).

DESCRIPTION: DURING EACH E-CLOCK CYCLE, THE OUTPUT COMPARE REGISTER 1 IS COMPARED TO THE FREE-RUNNING COUNTER.
IF THERE IS A COMPARE THEN:

1. THE INTERRUPT FLAG BIT IS SET

IN ADDITION, EITHER OR BOTH OF THE FOLLOWING MAY OCCUR:

1. THE STATE OF OUTPUT PINS OC7–OC0 MAY BE CHANGED

2. AN INTERRUPT MAY OCCUR

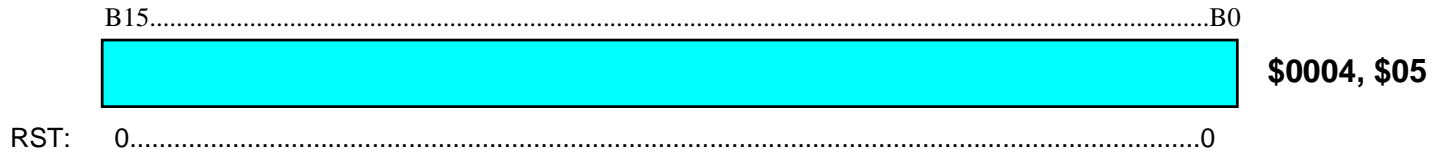
- OC7 CAN AFFECT MULTIPLE PINS (OC7–OC0)
- OC7 ACTION OVERRIDES ANY CONFLICTING OC7–OC0 ACTION FOR A GIVEN PIN.

Output Compare 7

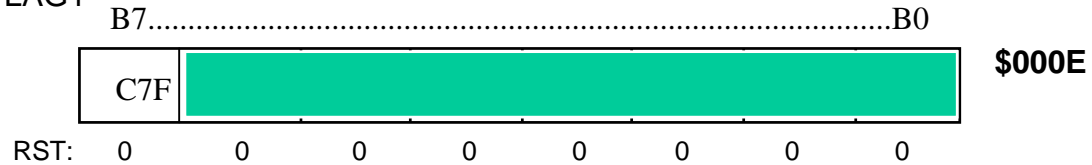
1 - **TC7** -16 BIT COMPARE REGISTER 7.

(2 of 2)

2. **TCNT** - 16-BIT TIMER



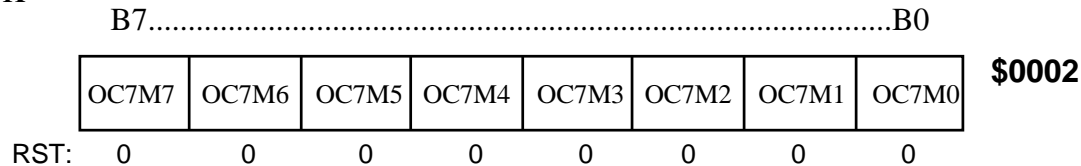
3. **TFLAG1** - TIMER FLAG1



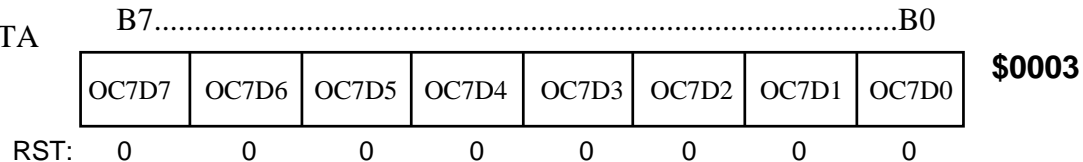
4. **TIE** - TIMER INTERRUPT ENABLE



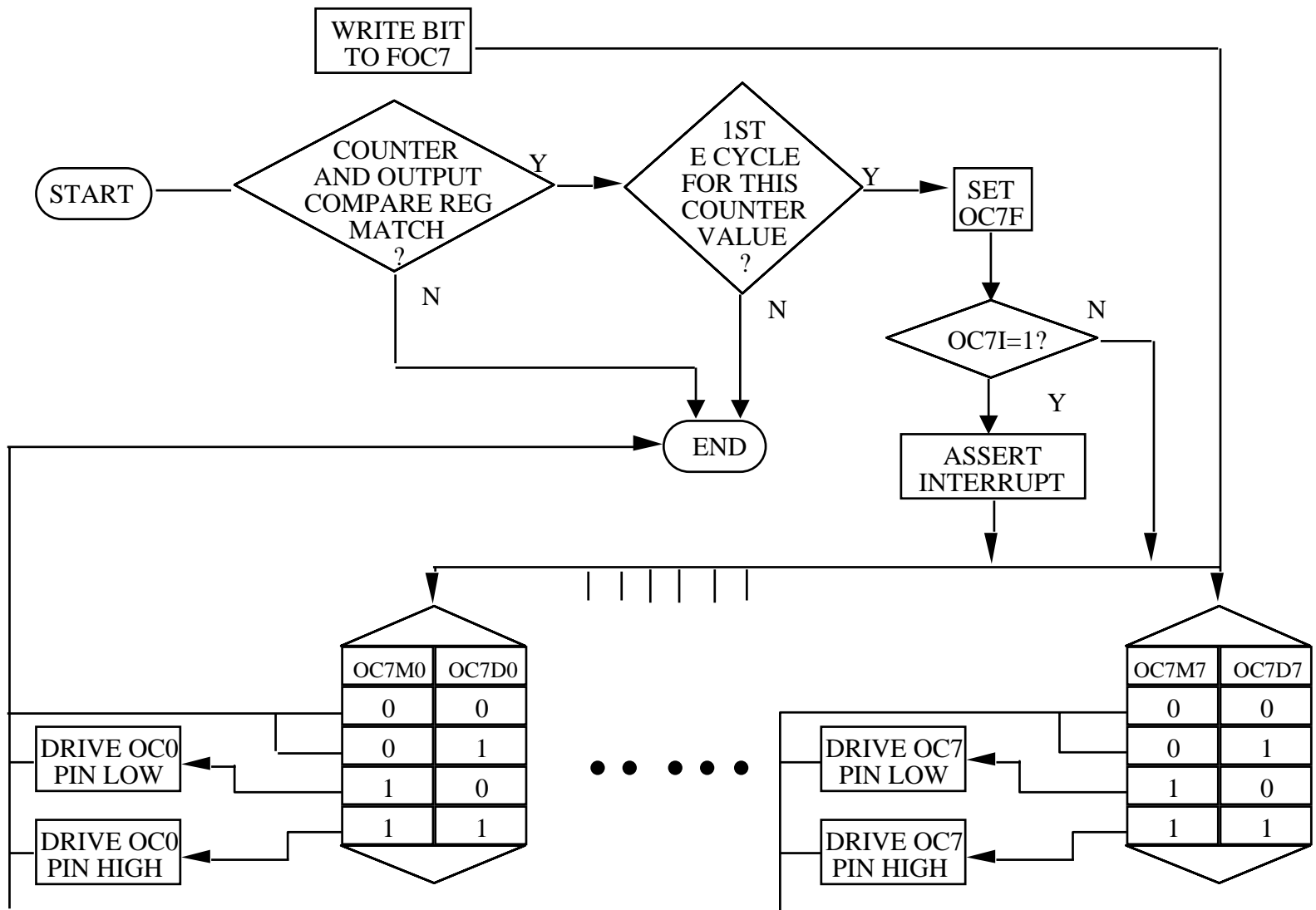
5. **OC7M** - OC7MASK



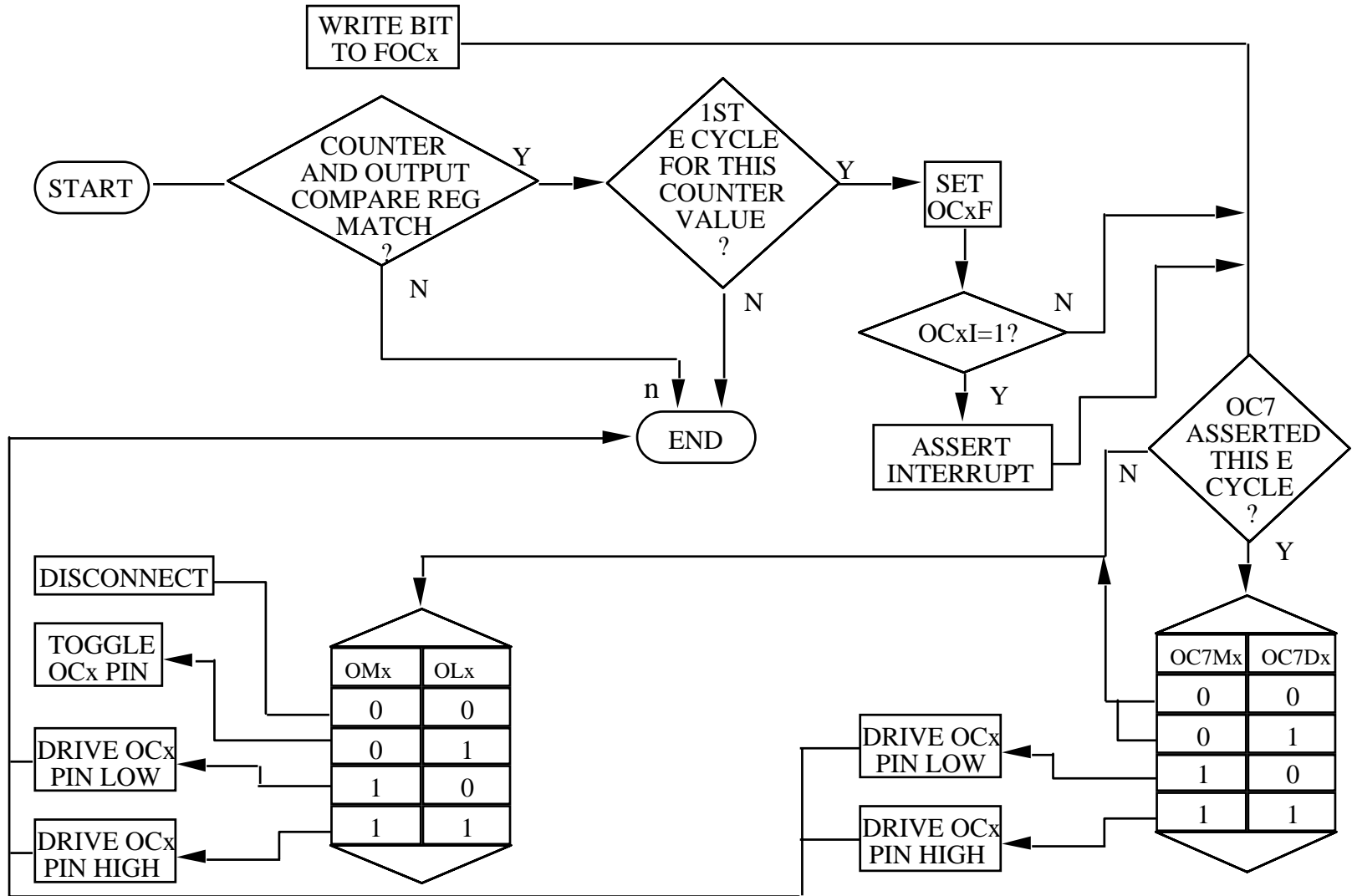
6. **OC7D** - OC7DATA



Output Compare 7 Flow Chart



Output Compare Flow Chart (Complete)



- FOR OC_x = OC7 – OC0

Timer Toggle on Overflow

TTOV -Timer Toggle On Overflow Register

TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0	Address Offset
								\$0007

RST: 0.....0

TOV_x - TOGGLE ON TIMER OVERFLOW

**TOV_x Toggles output compare pin on overflow.
This feature is applicable only when channel is
configured for Output Compare Function.**

Timer Output Compare Exercise

; Timer lab - outputs 1 to 8 channels of PWM out of Port T

```
main:      org      $4000

; use all channels as output compare function

; disable timer, operate in wait, continue in BDM
; fast clear enables

; enable clear of OCn when match on all channels

; disable Interrupts

; disable pull-ups, normal drive, TCNT reset by OC7
; set prescaler to divide-by-4

; set the OC7 to be an output port

; enable OC7 to set the output compare pins to high

; OC7 is the period of the PWM

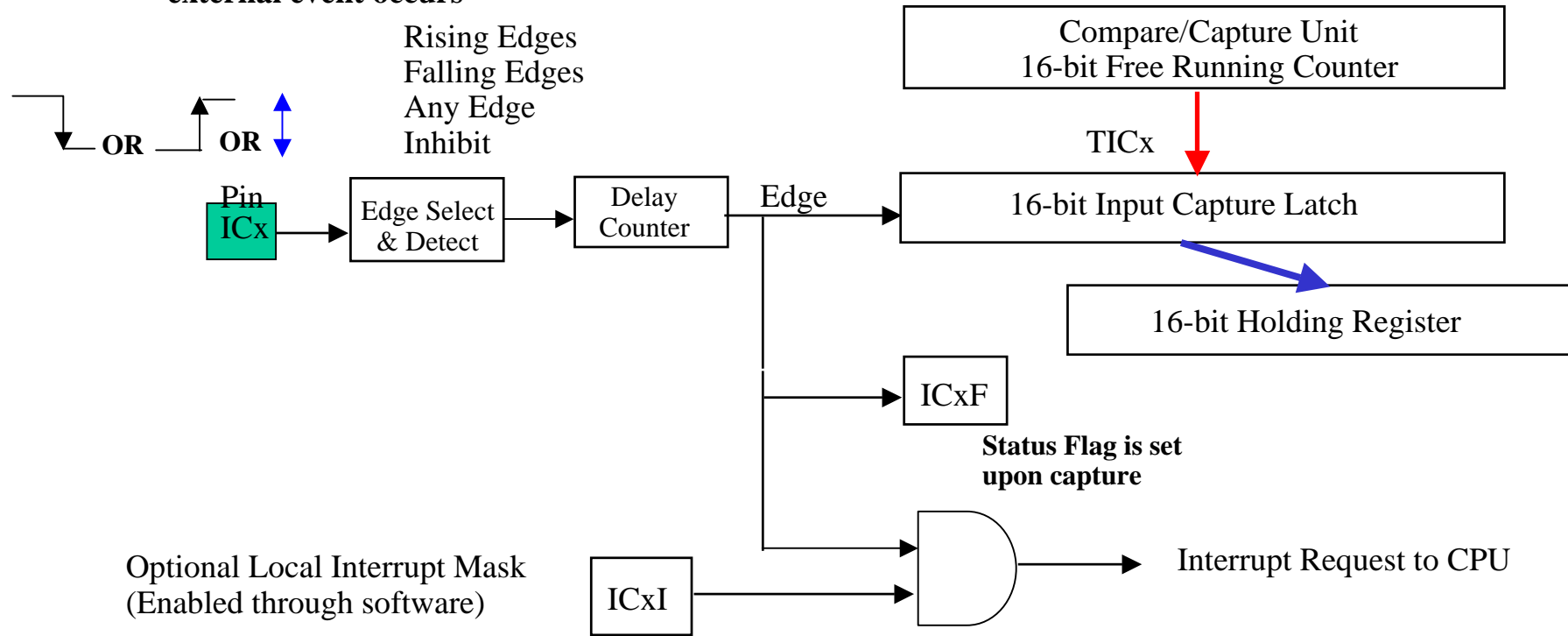
; OC0 is high for 32 clocks
; OC1 is high for 64 clocks
; OC2 is high for 128 clocks
; OC3 is high for 256 clocks
; OC4 is high for 512 clocks
; OC5 is high for 1024 clocks
; OC6 is high for 2048 clocks

; ready to go, now enable the timer

loop:      ; wait here
```

Input Capture Function

- Provides a mechanism to capture the time at which an external event occurs



- Up to 8 separate Input Capture function, IC7 - IC0
- Each Input Capture Function has its own Vector and Controls

DLYCT - Delay Counter Control Register

Bit 7	6	5	4	3	2	1	0	Address Offset
0	0	0	0	0	0	DLY1	DLY0	\$0029

- Examples: ABS braking. Radar distance measurement. Heart rate monitoring.

Note: Delay Counter produces a Pulse at preset clock count if the level of the input signal is the opposite of the level before the transition.

DLY[1:0] - Delay Counter Values

- 00 = Disabled
- 01 = 256 M Clocks
- 10 = 512 M Clocks
- 11 = 1024 M Clocks

Input Capture, IC7-IC0

(1 of 3)

USEFUL FOR:

- 1. MEASURING TIME BETWEEN EVENTS (OCCURING IN HARDWARE)**
- 2. REACTING TO REAL-TIME EVENTS**

DESCRIPTION: INPUT CAPTURE EDGE DETECTORS SENSE WHEN AN EDGE OCCURS ON THE PIN.

IF AN EDGE OCCURS, THE FOLLOWING MAY HAPPEN:

- 1. THE COUNTER VALUE GOES INTO THE INPUT CAPTURE REGISTER; A STATUS FLAG IS SET.**
- 2. AN INTERRUPT IS GENERATED TO CPU, IF Enabled.**

Input Capture, IC7-IC0 (2 of 3)

1. TC7 – TC0

16 BIT CAPTURE COMPARE REGISTER (TC7)

Address Offset

\$0010 - \$0011

-

-

16 BIT CAPTURE COMPARE REGISTER (TC0)

\$001E - \$001F

2. TFLG1

C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
-----	-----	-----	-----	-----	-----	-----	-----

\$000E

RST: 0 0 0 0 0 0 0 0

COMPARE/CAPTURE FLAGS
Write '1' to Clear Interrupt Flag

B7 B6 B5 B4 B3 B2 B1 B0

3. TMSK1

C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
-----	-----	-----	-----	-----	-----	-----	-----

\$000C

RST: 0 0 0 0 0 0 0 0

COMPARE/ CAPTURE MASK
0 = Interrupt Request Masked
1 = Interrupt Request Enabled

B7 B6 B5 B4 B3 B2 B1 B0

4. TCTL3

EDG7B EDG7A	EDG6B EDG6A	EDG5B EDG5A	EDG4B EDG4A
-------------	-------------	-------------	-------------

\$000A

RST: 0 0 0 0 0 0 0 0

Input Capture Edge
Control (IC7-IC0)

5. TCTL4

EDG3B EDG3A	EDG2B EDG2A	EDG1B EDG1A	EDG0B EDG0A
-------------	-------------	-------------	-------------

\$000B

RST: 0 0 0 0 0 0 0 0

EDGxB	EDGxA	ICx EDGE
0	0	No Edge – ICx Disab
0	1	Rising Edges Only
1	0	Falling Edges Only
1	1	Any Edge

Input Capture, IC7-IC0

(3 of 3)

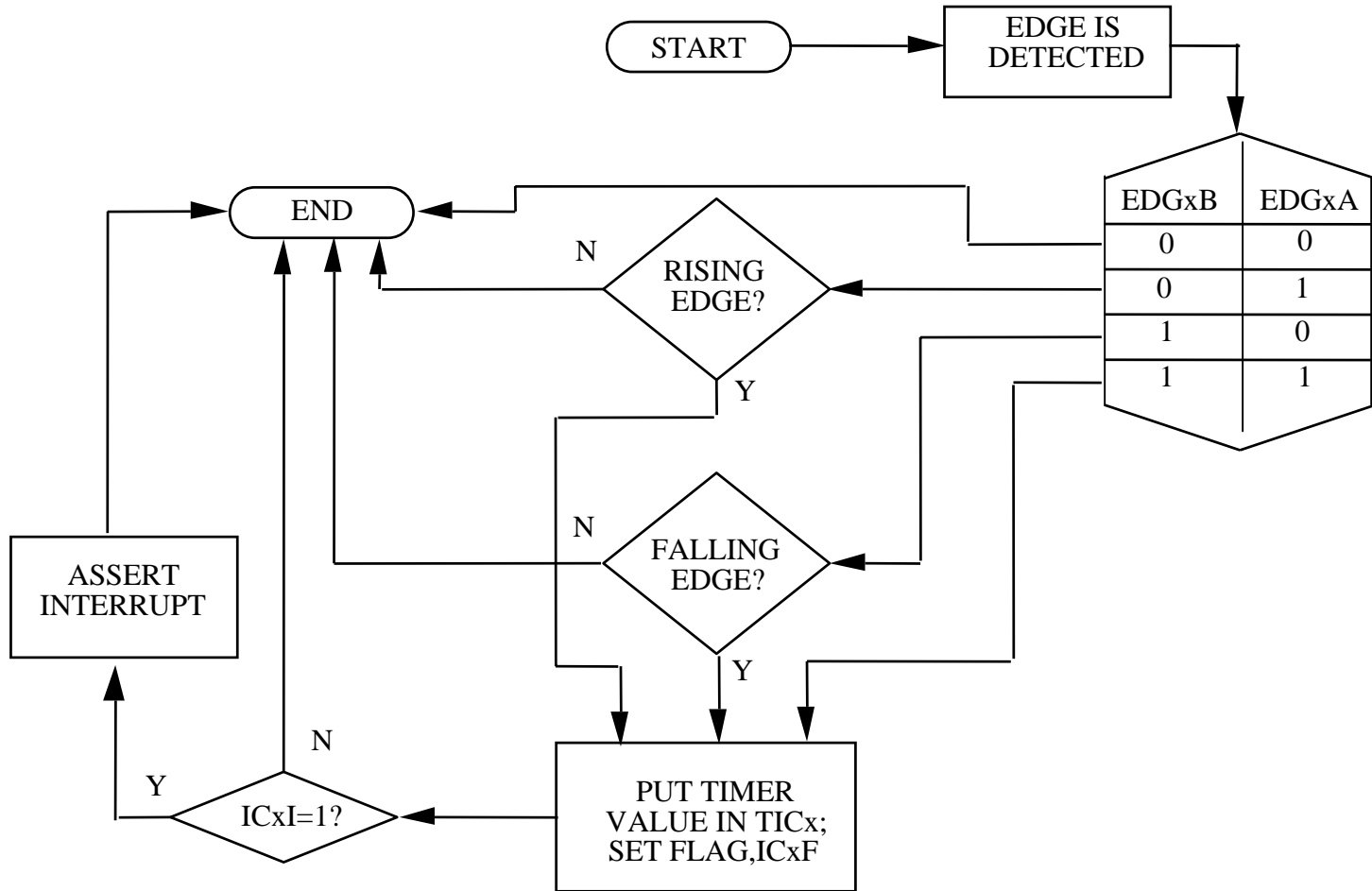
INTERRUPTS: FOR INPUT CAPTURES IC7 – IC0

- TO CLEAR INTERRUPT, WRITE 1 TO ICxF BIT IN TFLG1
DO NOT USE BIT MANIPULATION INSTRUCTIONS (SINCE RM/W OPERATION)
- IC7–IC0 VECTORS ARE USED.

RESET CONDITIONS:

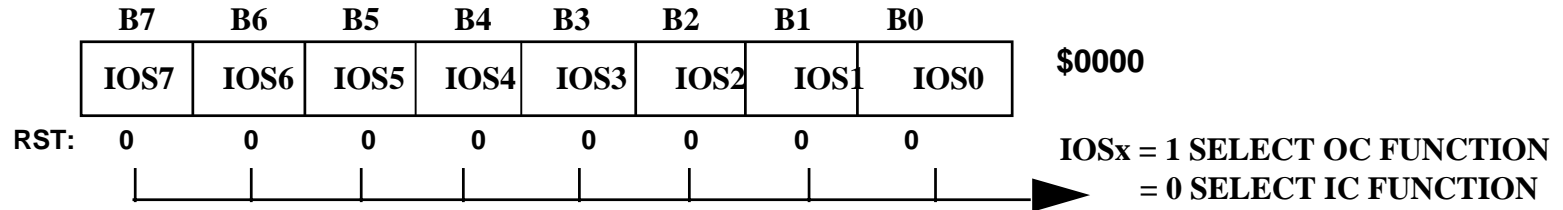
- INPUT CAPTURE FUNCTIONS ARE DISCONNECTED FROM INPUT CAPTURE PINS
- INTERRUPTS ARE DISABLED
- FLAG BITS ARE CLEARED

Input Capture Flow Chart

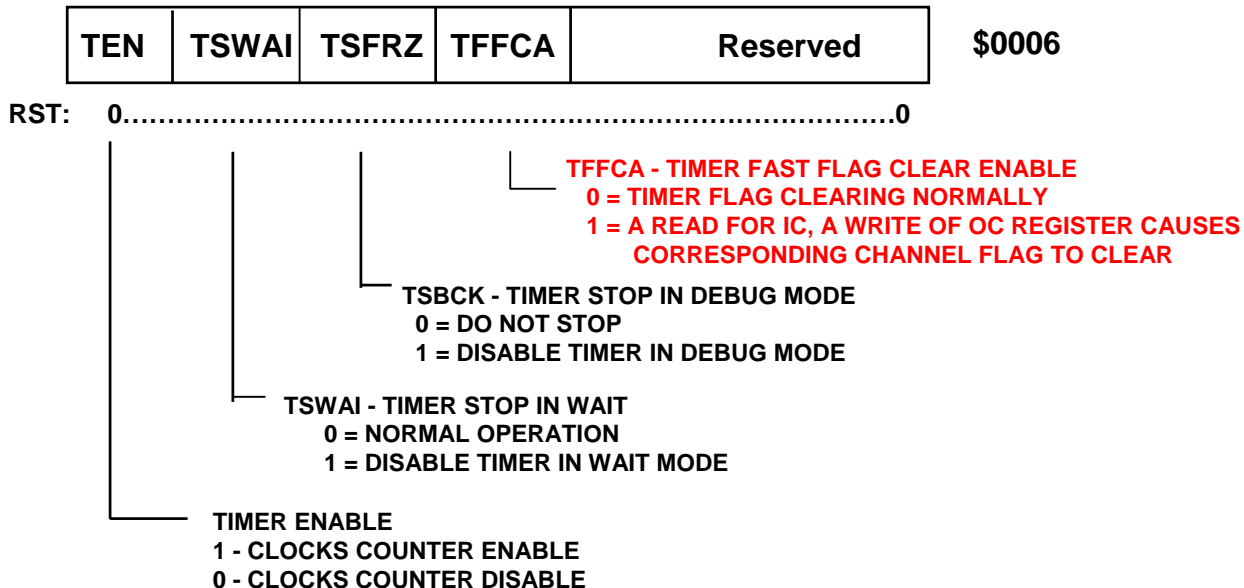


IC/OC Select

TIOS - TIMER INPUT CAPTURE/OUTPUT COMPARE SELECT REGISTER



TSCR - TIMER SYSTEM CONTROL REGISTER



Timer Input Capture Lab

Write a routine to measure the period of a square wave on TC1. The routine uses the Input Capture to measure the period from one rising edge to the next. Use software polling routine, non-Interrupt-driven. Assume system clock is 25MHZ, set the Timer prescaler to divide by 4.

TIME1	EQU	\$1200
DIFF	EQU	\$1202
	ORG	\$4000

ADDRESS OF TIME1
ADDRESS OF DIFFERENCE

PROGRAM BEGINS HERE

1. Load X register with register block address
2. Configure channel 1 for input capture (write TIOS)
3. Set TCTL4 to capture rising edge on channel 1.
4. Disable Ch1 Interrupts in TMSK2
5. Enable and start timer
6. Read Timer status register into Accumulator
7. Clear Timer Ch1 status flag C1F.
8. Wait here until C1F is set, else go to 9.
9. Load captured value into Accumulator D.
10. Store D to Ram in TIME1
11. Clear C1F by writing a 1 to it
12. Wait here until C1F is set, else go to 13.
13. Load captured value into Accumulator D.
14. Subtract TIME1 from D
15. Store D to Ram in DIFF location.
16. Return from subroutine

Pulse Accumulator

USEFUL FOR:

- 1. EVENT COUNTING**
- 2. GATED TIME ACCUMULATION**

DESCRIPTION:

IF PULSE ACCUMULATION IS Enabled, THEN HCS12 RESPONDS TO EDGES ON PAI BY INCREMENTING THE 8 OR 16-BIT PULSE Accumulator COUNTER.

EVENT COUNTING MODE:

INPUT EDGES ON PAI INCREMENT THE 8/16-BIT COUNTER

GATED TIME ACCUMULATION MODE:

THE 8/16-BIT COUNTER IS INCREMENTED BY AN E/64 CLOCK IF Enabled BY THE LAST EDGE ON PAI

IF THE SPECIFIED EDGE OCCURS, THEN:

- 1. THE PULSE Accumulator FLAG BIT IS SET**

IN ADDITION, THE FOLLOWING MAY OCCUR:

- 1. THE COUNTER MAY BE INCREMENTED**
- 2. THE PULSE Accumulator OVERFLOW BIT MAY SET**
- 3. AN INTERRUPT IS GENERATED TO CPU, IF Enabled.**

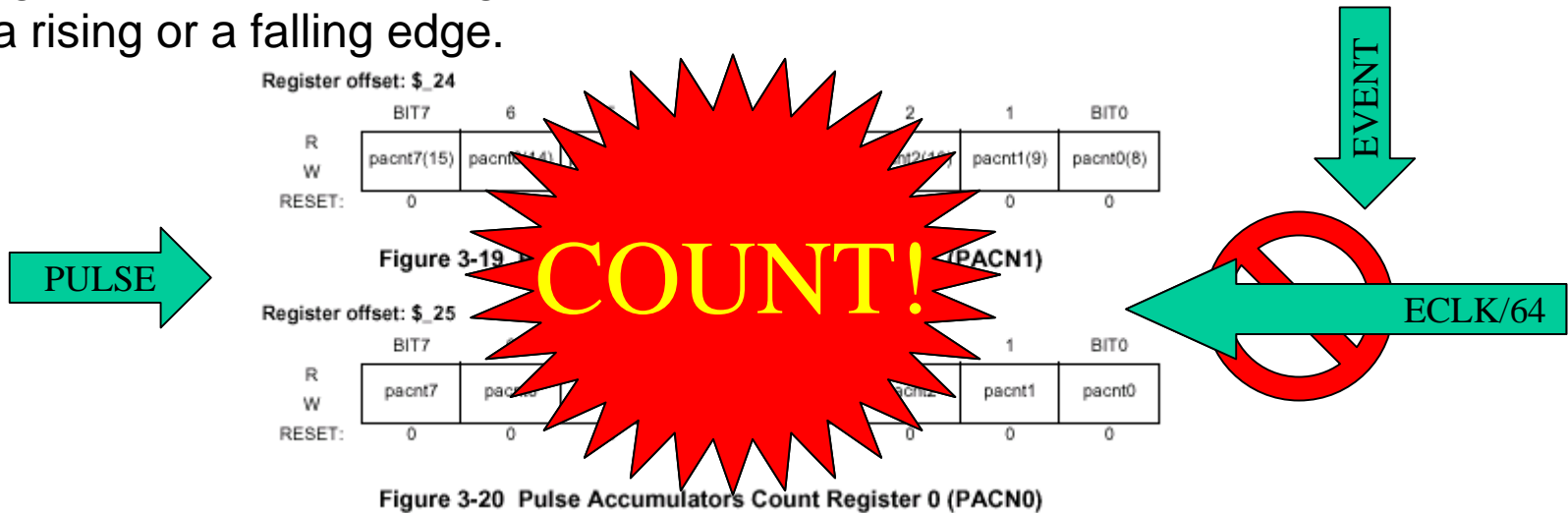
Pulse Accumulator

Event Counter Mode

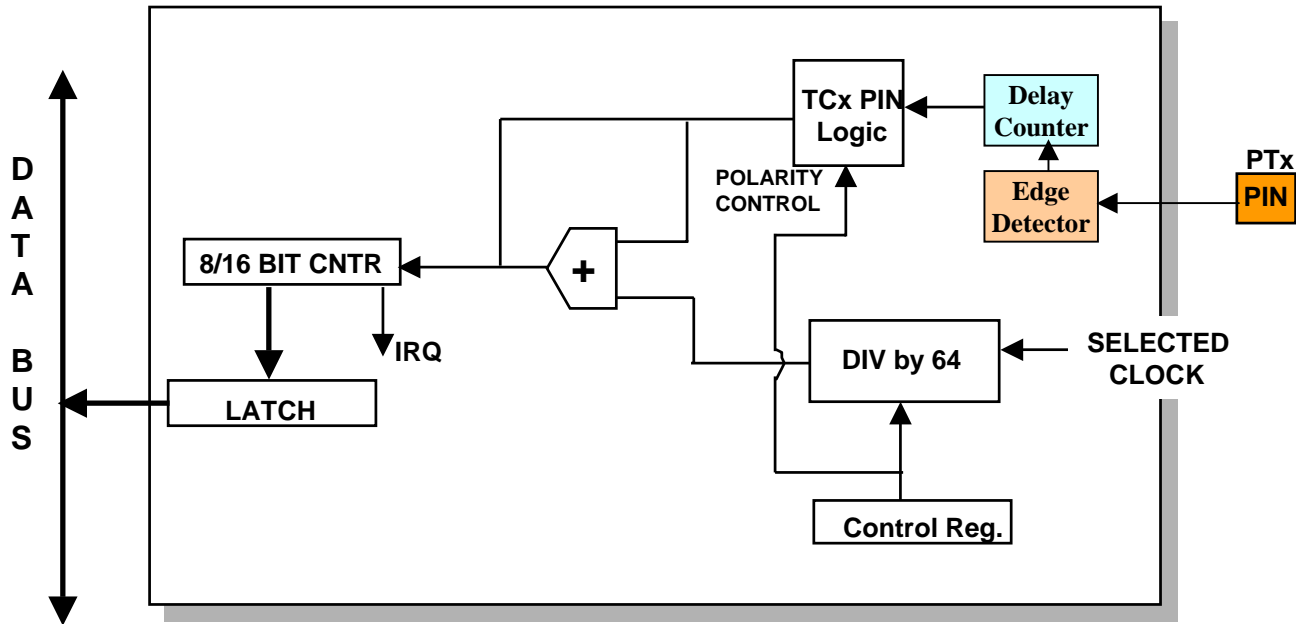
- Pulse accumulator is an event counter. An event is a prescribed external pulse applied to the relative MCU pin.
- Each pulse increments the value of the pulse accumulator register.
- Trigger event can be configured as a rising or a falling edge.

Gated Accumulation Mode

- Pulse accumulator is an event **length** counter. Counter records the length of a pulse applied on the relative MCU pin.
- The MCU internal bus clock is divided by 64 and applied to the pulse accumulator for the duration of the external event.
- Trigger event is configurable as a logic high event or a logic low event.



Pulse Accumulator Block Diagram



DLYCT - Delay Counter Control Register

Bit 7	6	5	4	3	2	1	0	Address Offset
0	0	0	0	0	0	DLY1	DLY0	\$0029

DLY[1:0] - Delay Counter Values

- 00 = Disabled
- 01 = 256 M Clocks
- 10 = 512 M Clocks
- 11 = 1024 M Clocks

Note 1: PTx may be used as Pulse Accumulator, Input Capture or Output Compare pin.

Where $PTx = PT0 - PT3$

Note 2: Delay Counter produces a Pulse at preset clock count if the level of the input signal is the opposite of the level before the transition.

PA Registers (1 of 2)

Pulse Accumulator Count Registers

Address Offset

PACN3	Bit 7	6	5	4	3	2	1	Bit 0	\$0022
PACN2	Bit 7	6	5	4	3	2	1	Bit 0	\$0023
	0	0	0	0	0	0	0	0	
PACN1	Bit 7	6	5	4	3	2	1	Bit 0	\$0024
PACN0	Bit 7	6	5	4	3	2	1	Bit 0	\$0025
	0	0	0	0	0	0	0	0	

ICPAR - Input Control pulse Accumulator Register

	Bit 7	6	5	4	3	2	1	Bit 0	
	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN	\$0028
RESET	0	0	0	0	0	0	0	0	

PAXEN - PAX Enable

Pulse Accumulator Holding Registers

PA3H	Bit 7	6	5	4	3	2	1	Bit 0	\$0032
PA2H	Bit 7	6	5	4	3	2	1	Bit 0	\$0033
PA1H	Bit 7	6	5	4	3	2	1	Bit 0	\$0034
PA0H	Bit 7	6	5	4	3	2	1	Bit 0	\$0035
	0	0	0	0	0	0	0	0	

PAXH - Used to latch PAX when enabled

PA3H - PA0H Registers are read only

PA Registers (2 of 2)

PACTL - PA Control Register

Address Offset

\$0020

	Bit 7	6	5	4	3	2	1	Bit 0
	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
RESET:	0	0	0	0	0	0	0	0

PAEN - PA Enable

1 = Pulse Accumulator Enabled

0 = Pulse Accumulator Disabled

PAOVI - PA Overflow Interrupt Enable

1 = PAO Interrupt Enabled

0 = PAO Interrupt Disabled

PAI - PA Input Interrupt Enable

1 = PAI Interrupt Enabled

0 = PAI Interrupt Disabled

Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

Clock Selection

CLK1	CLK0	Clock Source
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

PAFLG - PA Interrupt Flag Register

Address Offset

\$0021

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	0	PAOVF	PAIF
RESET:	0	0	0	0	0	0	0	0

PAOVF -- Pulse Accumulator Overflow Flag

Sets when PA overflows from \$FF to \$00

PAIF - Pulse Accumulator Input Flag

Sets when the programmed transition is detected on PA Pin.

Pulse Accumulator

Interrupts: For Pulse Accumulator Input and Pulse Accumulator Overflow.

- To clear Interrupt write a '1' to PAIF or PAOVF bits in TFLG2.
Do not use bit manipulation instructions (since RM/W operation).
- Pulse Accumulator or Pulse Accumulator Overflow vector used

Reset conditions:

- Pulse accumulator is disabled
- Event counter mode
- Falling edges(event counter mode) or PAI high enables
(gated time accumulation mode)
- Interrupts are disabled
- Flag bits are cleared

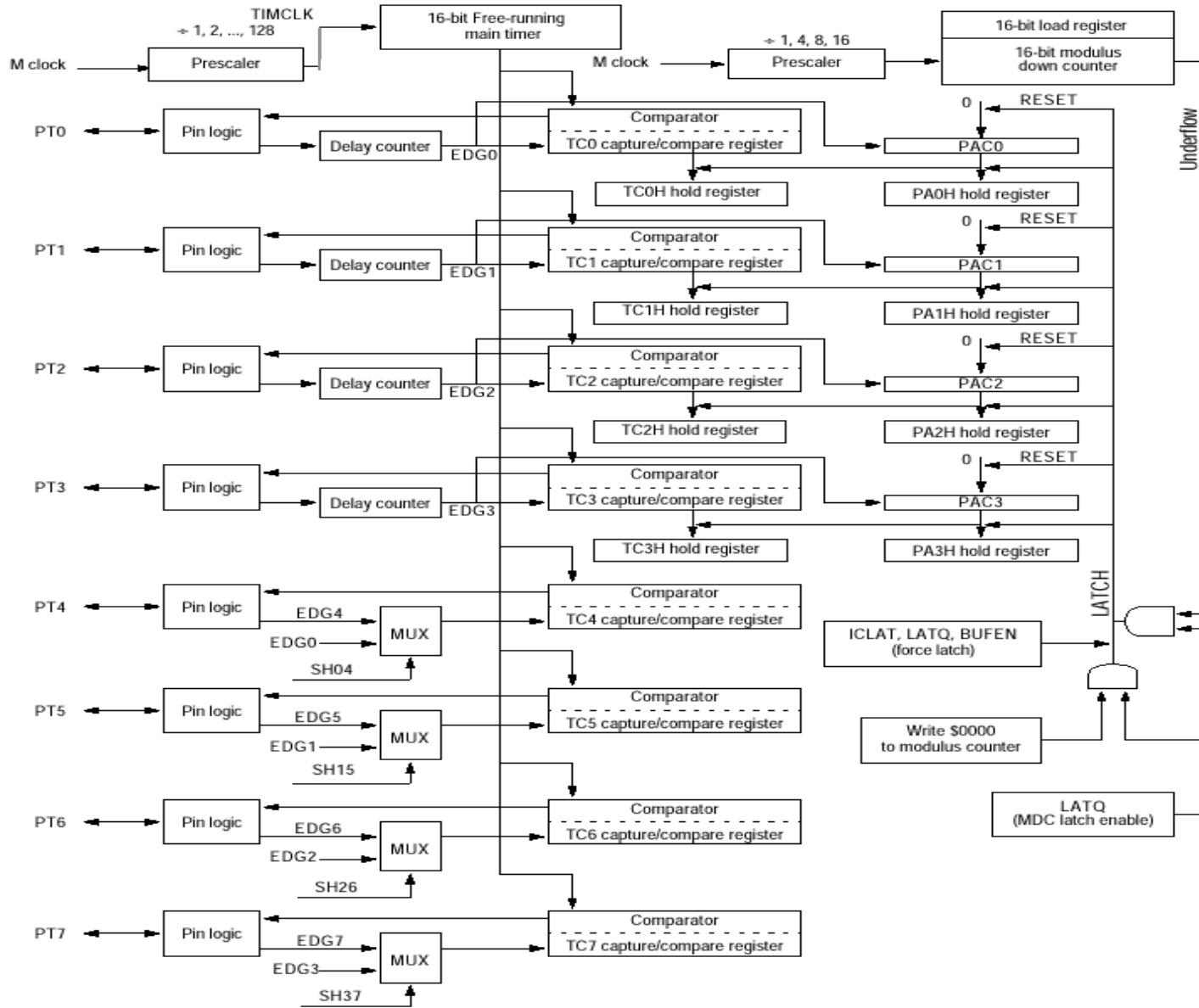
Pulse Accumulator Modes

- For event counting mode, PEDGE selects which PAI edge is used to increment the PACNT register.
- For gated accumulation mode, PEDGE selects which PAI state is used to inhibit counting.
(i.e. $\text{PEDGE} = 1 \rightarrow$ inhibit counting when $\text{PAI} = \text{HI}$).
- Since gated accumulation mode will only increment PACNT every 64 E clocks, waveforms with gated times less than 64 E clocks are not guaranteed to be detected.
- The measured gated time of any waveform is only accurate to within 64 E clocks for each counting state on the PAI pin.

ECT Latch & Queue

Modes

EC I Latch Mode

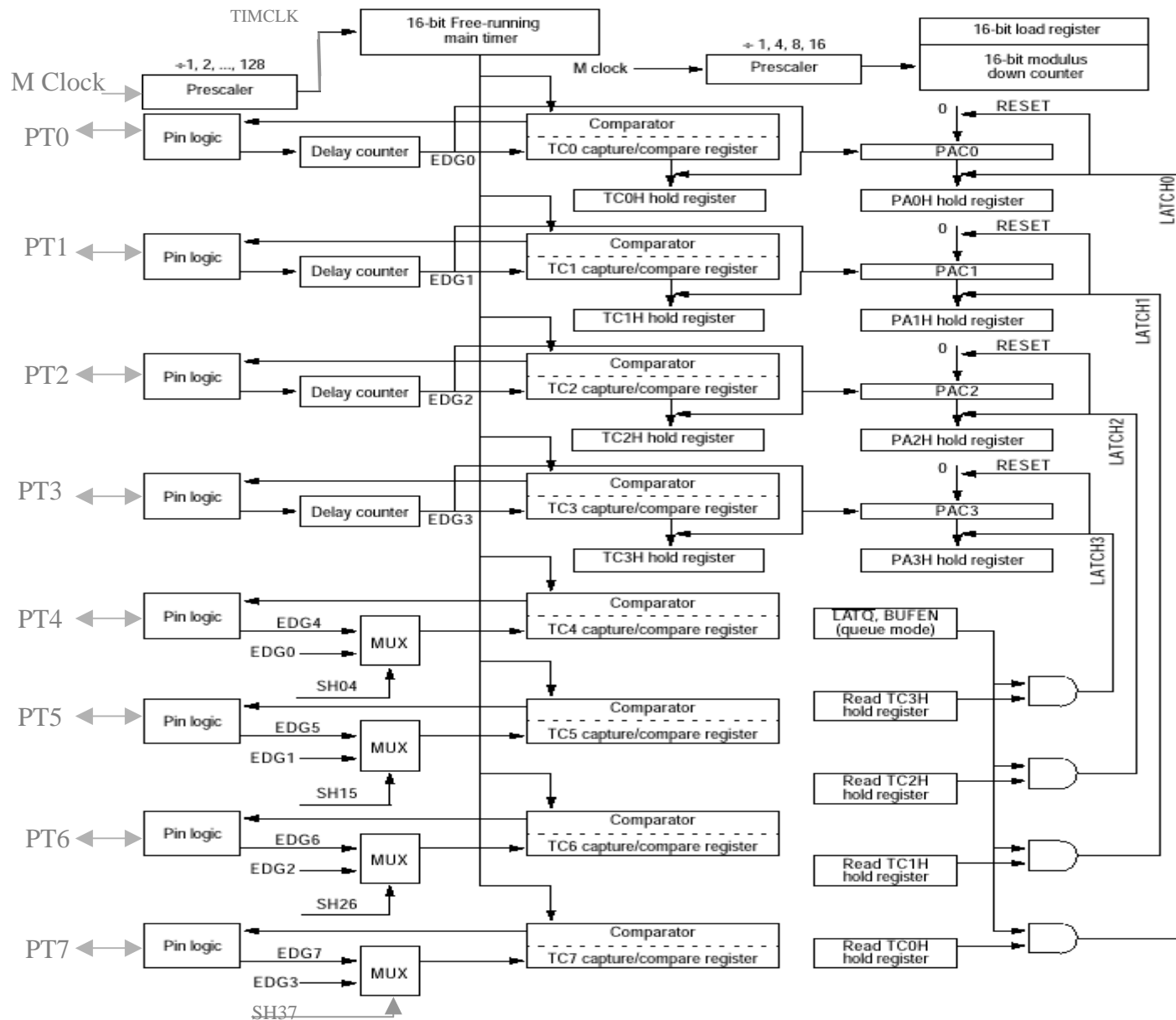


Latch Mode: LATQ = 1

Modulus Down-Counter causes IC x & PA x registers to transfer to their corresponding holding registers when Counter reaches \$0000, or when Down-Counter is written with \$0000..

In this mode, IC registers are transferred to their holding register when ICLAT bit is written in the MCCTL register

EC1 Queue Mode

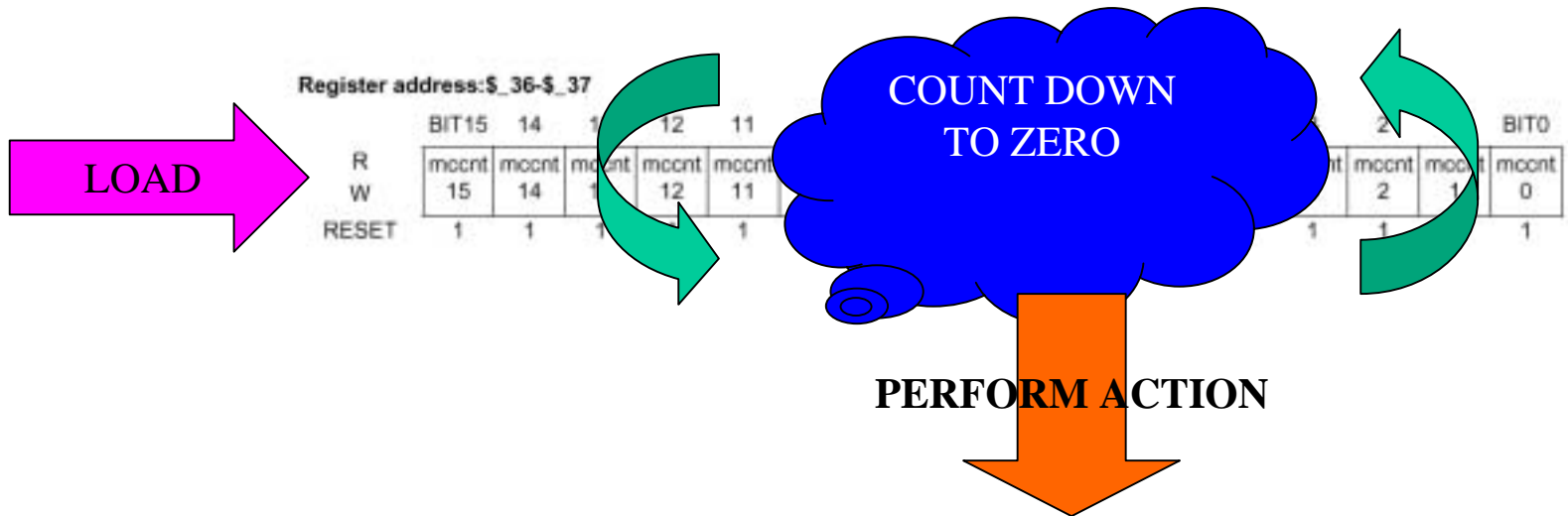


Queue Mode: LATQ = 0
An Input Capture x Event causes the IC register to transfer to corresponding Holding register and new captured value is written to corresponding IC register.

This mode also causes the PA x to transfer to its corresponding holding register when IC holding register x is read.

Modulus Down-Counter in this mode may only be used to generate periodic Interrupts.

Modulus Down-Counter



Binary down-counter. Full control over count start value.

Applications in accurate event timing - used to generate periodic flags and interrupts.

Runs independently of master timer. Clocked directly from the bus clock through a dedicated prescaler.

Can be set to generate flags /interrupts at a discrete time

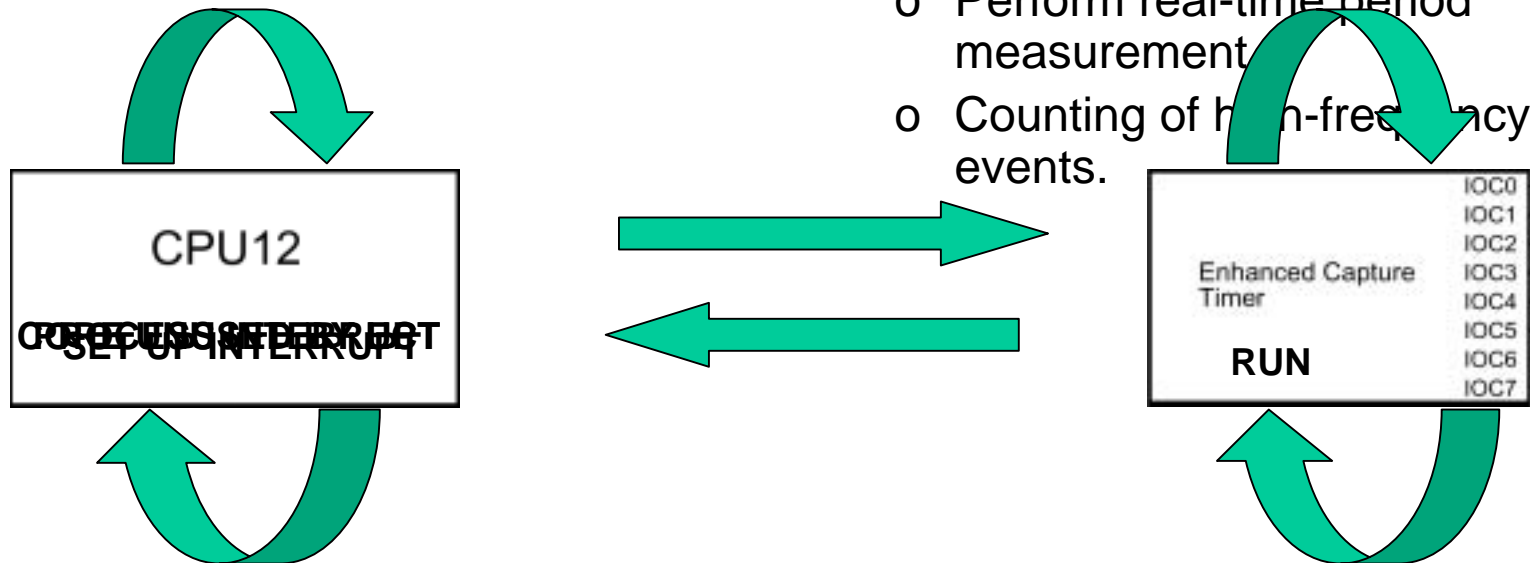
from activation, or set to reload the count start value upon reaching \$0000 (periodic modulus mode).

Parameter	Value	Units
<i>Crystal Frequency</i>	16	MHz
<i>Bus Frequency</i>	8	MHz
<i>Bus Tick Time</i>	125.0000	nS
<i>Periodic Interrupt Time</i>	191	uS
<i>Bus Ticks Required</i>	1528.00	Ticks
<i>Modulus Counter Prescaler</i>	4	
<i>Modulus Counter Start Value</i>	382	

ECT Interrupt Generation

Interrupt Source	Description
Timer Channel 7-0	Active high timer channel interrupts 7-0
Modulus counter underflow	Active high modulus counter interrupt
Pulse Accumulator B Overflow	Active high pulse accumulator B interrupt
Pulse Accumulator A Input	Active high pulse accumulator A input interrupt
Pulse Accumulator A Overflow	Pulse accumulator overflow interrupt
Timer Overflow	Timer Overflow interrupt

- ECT has thirteen discrete interrupt vectors - No need to continually poll critical status flags.
- Interrupts allow delegation and optimisation of core use.
- Extremely flexible. Examples of interrupt usage:
 - Launch routines at real-time fixed intervals.
 - Perform real-time period measurement
 - Counting of high-frequency events.



Enhanced Capture

Features on ECT module in addition to standard TIM module :-

- 16-bit buffer registers on four input capture channels.
- Four 8-bit / two 16-bit pulse accumulators.
- 16-bit modulus down-counter with 4-bit prescaler.
- Four user selectable delay counters for increased time immunity.
- Main timer prescaler extended to 7-bit.

EXTERNAL EVENT

Register offset: \$_04-\$_05

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt	tcnt
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Master Timer

COPY

READ DATA

TC0 — Timer Input Capture/Output Compare Register 0 Register offset: \$_10-\$_11

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Input Capture Register

READ DATA

COPY

Register offset: \$_38-\$_39

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Holding Register

Modulus Counter Registers

MCCNT - Modulus Down-Counter Count Register

Address Offset
\$0036, 37

Bit 15	14	13	12	11	10	9	Bit 8
Bit 7	6	5	4	3	2	1	Bit 0

RESET: 1 1 1 1 1 1 1 1

*Modulus Down-Counter may be used to generate periodic Interrupts.
It can also be used to latch IC and PA registers to their holding registers.*

MCCTL - Modulus Down-Counter Control Register

Address Offset
\$0026

Bit 7	6	5	4	3	2	1	Bit 0
MCZI	MODMC	RDMCL	ICLAT	FLMC	MCEN	MCPR1	MCPR0

RESET: 0 0 0 0 0 0 0 0

MCZI - Modulus Counter Interrupt Enable

MODMC - Modulus Mode Enable

1 = Counter is loaded with last value written to Modulus Count Register.
0 = Counter counts once from value written to it and will stop at \$0000.

RDMCL - Read Modulus Down Counter Load

1 = Reads of Counter returns the contents of the Load Register.
0 = Read of Counter returns current value of the present count.

ICLAT - Input Capture Force Latch Action

When Latch Mode is enabled, write '1' to this bit causes IC3-IC0 and their corresponding Pulse Accumulators to be latched into their associate holding registers.

FLMC - Force Load Register into Modulus Counter by writing '1' to this bit

MCEN - Modulus Down-Counter Enable

1 = Modulus Counter Enabled.
0 = Modulus Counter Disabled.

MCPR[1:0] - Modulus Counter Prescaler Select

00 = Div/1
01 = Div/4
10 = Div/8
11 = Div/16

MCFLG - Modulus Down-Counter Flag Register

Address Offset
\$0027

Bit 7	6	5	4	3	2	1	Bit 0
MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0

RESET: 0 0 0 0 0 0 0 0

MCZF - Modulus Counter Underflow Interrupt Flag.
This Flag is set when Modulus Counter reaches \$0000.
Write '1' to clear.

POLF{3:0} - First Input Capture Polarity Status

1 = Input Capture x was caused by rising edge.
0 = Input Capture x was caused by falling edge.

Where x = IC3 - IC0.

EC Control Registers

ICSYS - Input Control System Register

	Bit 7	6	5	4	3	2	1	Bit 0	Address Offset
	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ	\$002B
RESET:	0	0	0	0	0	0	0	0	

SH_{xy} — Share Input action of Input Capture Channels x and y

1 = The channel input 'x' causes the same action on the channel 'y'. The port pin 'x' and the corresponding edge detector is used to be active on the channel 'y'.

0 = Normal operation

TFMOD — Timer Flag-setting Mode

Allows a timer Interrupt to be generated after capturing two values in the capture and holding registers instead of generating an Interrupt for every capture.

1 = If in Queue mode, timer flags C3F-C0F are set when a latch on the corresponding holding register occurs.

0 = C3F -C0F are when a valid edge occurs on corresponding IC timer pin.

PACMX - 8-Bit pulse Accumulator Max Count

1 = When PA reaches the value \$FF, it will not increment further.
0 = PA will overflow to \$00.

Note: For PACMX = 1, when count is read as \$FF, it indicate a count of 255 or more.

BUFEN -IC Buffer Enable

1 = IC & PA Holding Registers are enabled.
0 = IC & PA Holding Registers are disabled.

LATQ = Input Control Latch or Queue Mode Enable

1 = Latch mode is enabled.
0 = Queue Mode is enabled.

ICOVW - Input Control Overwrite Register

	Bit 7	6	5	4	3	2	1	Bit 0	Address Offset
	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0	\$002A
RESET:	0	0	0	0	0	0	0	0	

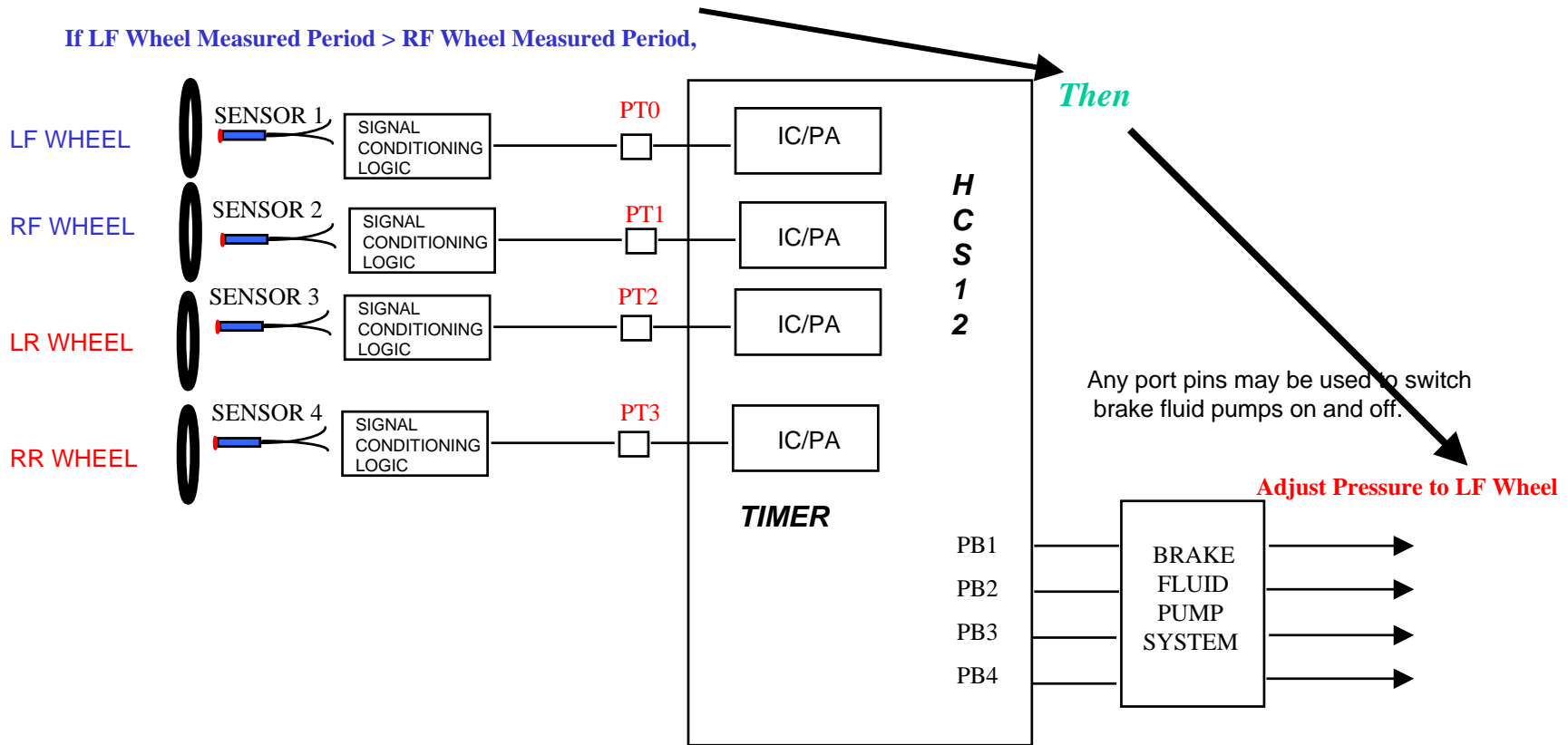
NOVW_x - No Input Capture Overwrite

These control bits prevent an overwrite to the IC x registers until read or latched in the holding register

1 = The related IC or Holding register will not be overwritten unless read or latched.

0 = The related Capture register will be overwritten when a new input capture or latch occurs.

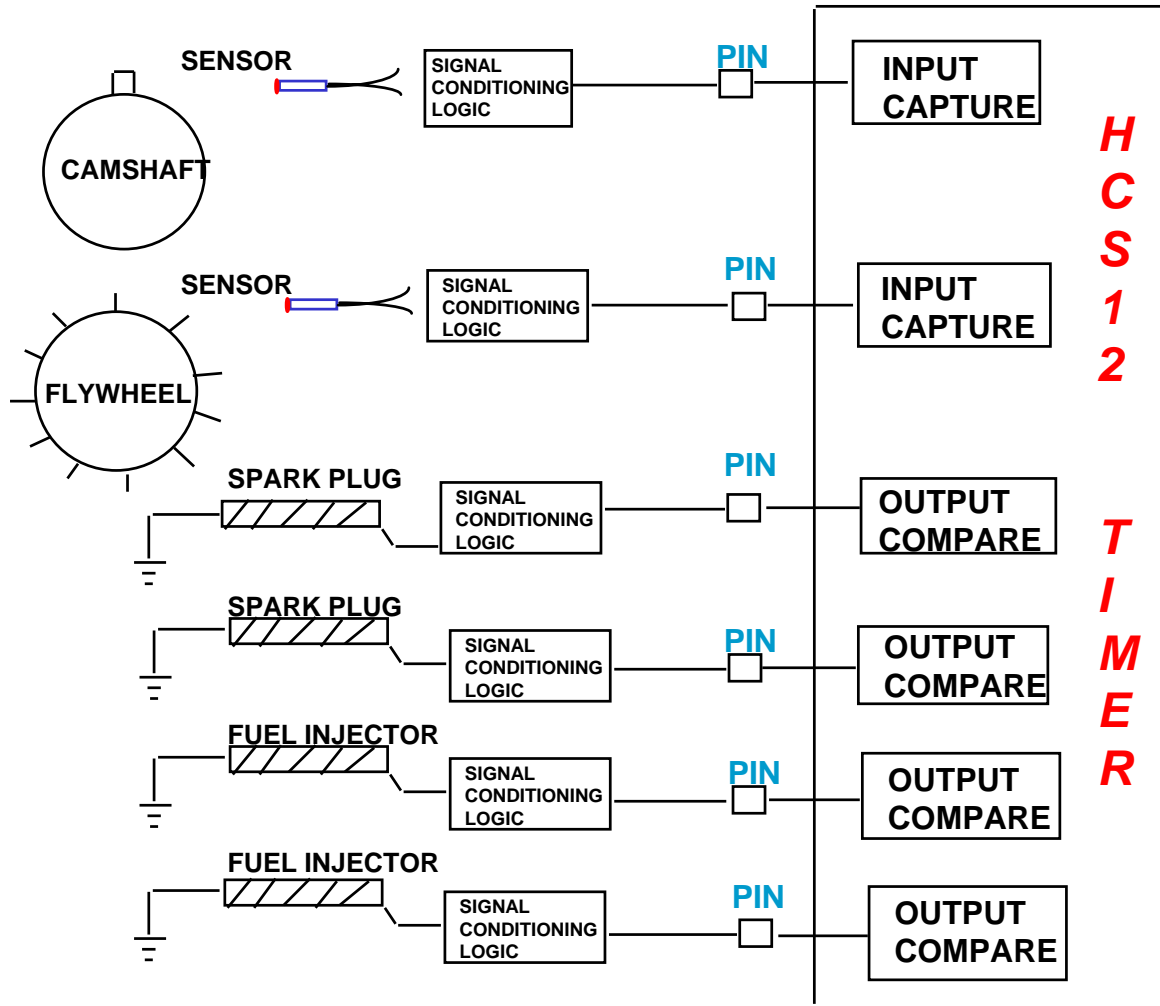
ABS Application Example



- Timer Input Captures measure wheel rotation.
- Send commands to brake fluid pumps to adjust pressure.

Angle Based Engine Control

Application Example



TIMER FUNCTIONS CONCLUSION

Timer

Output Compare

Input Capture

Pulse Accumulator

Latch & Queue Modes